University of Bahrain
College of Information technology
Department of Computer Engineering

Test (2)

Student Name	
I.D. No.	
Section	

Course Title: Digital Logic
Course number: ITCE 202-ITCE 250
Semester: 1
Academic Year: 2012/2013
Duration : 1 hour
Date: 23rd December 2012

Model Answer

Read the following before you start:
1. Write your name, ID and section number
2. Answer all questions.
3. Write your answers on the attached sheets only.

Question	Mark	Mark attained
1	25	
2	25	
3	25	
4	25	
Total	100	

Question [1]: [25 mark]

a- Give the truth table and the output' equations Sum= f(a,b,cin) and Cout= f(a,b,cin) of a Full Adder.

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A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$Sum = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

$= \bar{A}(B\bar{C} + \bar{B}C) + A(\overline{B\bar{C} + \bar{B}C})$

$= \bar{A}(B \oplus C) + A(\overline{B \oplus C})$

$= A \oplus B \oplus C$ →

$Cout = AB + AC_{in} + BC_{in}$ →

Sum

Á \ A	0	1
0	0	1
1	0	1

Cout

Á \ A	0	1
0	0	1
1	1	1

b- Give the truth table and the output' equations Sum=f(a,b) and Cout=f(a,b) of a Half Adder.

A	B	Sum	Cout
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

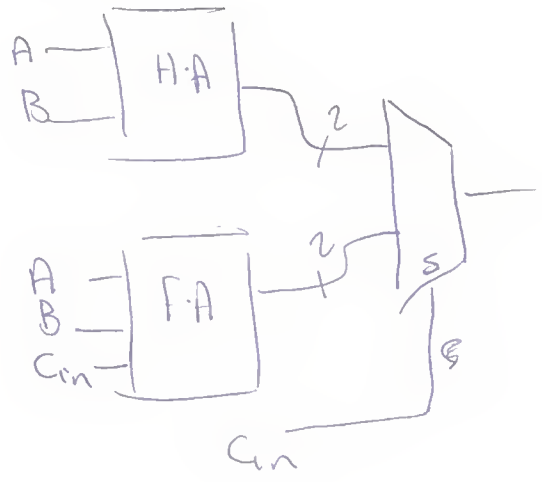
$Sum = \bar{A}B + A\bar{B}$

$= A \oplus B$ →

$Cout = AB$ →

Á \ A	0	1
0	0	1
1	1	1

c- We want to design a circuit that performs an addition of binary bits (a, b and cin) by using a Full or Half Adders. The bit cin is used to select the Full or the Half adders outputs. Give the design and show the different required connections.



Question [2] : [25 mark]

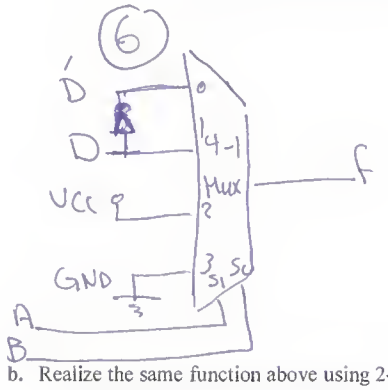
a. Realize the following function using 4-to-1 Multiplexer with minimum number of additional logic gates, and by using A and B as a selectors, where S_1=A & S_0=B:

$$F(A,B,C,D) = AB' + A'BD + B'D'$$

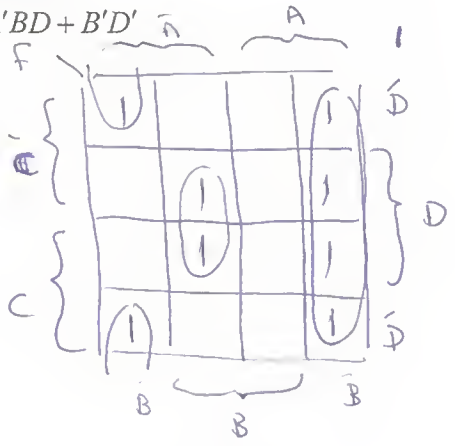
$f(A,B,C,D) = \bar{A}\bar{B}(D) + \bar{A}B(D) + A\bar{B}(1) + AB(0)$

(10)

(6)



(4)

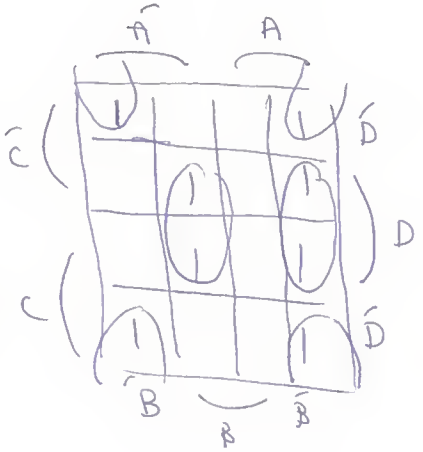


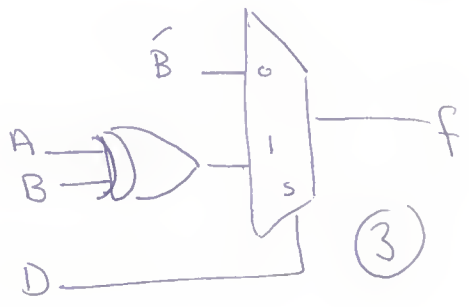
b. Realize the same function above using 2-to-1 Multiplexer with minimum number of additional logic gates, and by using D as a selector.

$f(A,B,C,D) = \bar{D}(\bar{B}) + D(A\bar{B} + \bar{A}B)$

$= \bar{D}(\bar{B}) + D(A \oplus B)$

(2)





(3)

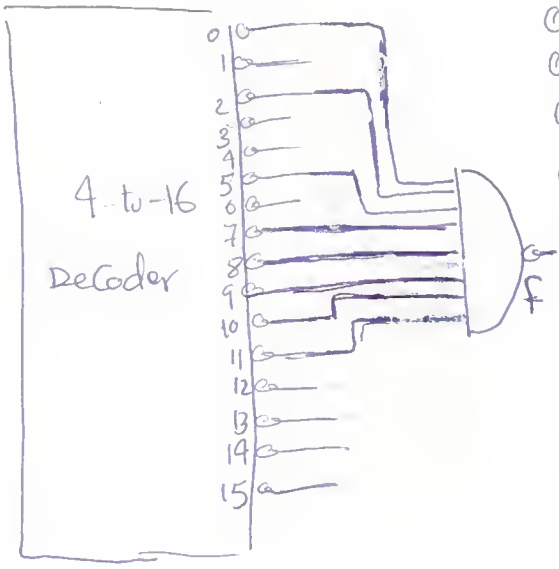
(10)

c. Realize the same function above using 4-16 decoder with inverted outputs and other additional logic gates.

(3)

A	B	C	D	F
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

(7)



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Question [3]: [25 mark]

a. Write the truth table of a J-K FF, and derive the characteristic (next-state) equation.

J	K	Q
0	0	Q
0	1	0
1	0	1
1	1	$\bar{Q}$

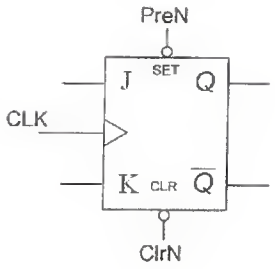
J	K	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

KQ \ J	0	1
00	0	1
01	1	1
11	0	0
10	1	1

$$Q^+_{JK} = J\bar{Q} + \bar{K}Q$$

5 5 2 5

i. Complete the given flip flop operation table for the given J-K FF.



CLK	J	K	PreN	ClrN	Q
x	x	x	0	0	not allowed
x	x	x	0	1	1
x	x	x	1	0	0
↓	0	0	1	1	Q
↓	0	1	1	1	0
↓	1	0	1	1	1
↓	1	1	1	1	$\bar{Q}$
0, 1, ↑	x	x	1	1	Q

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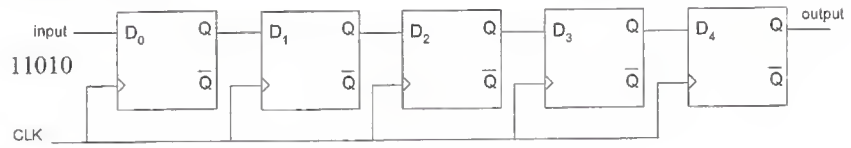
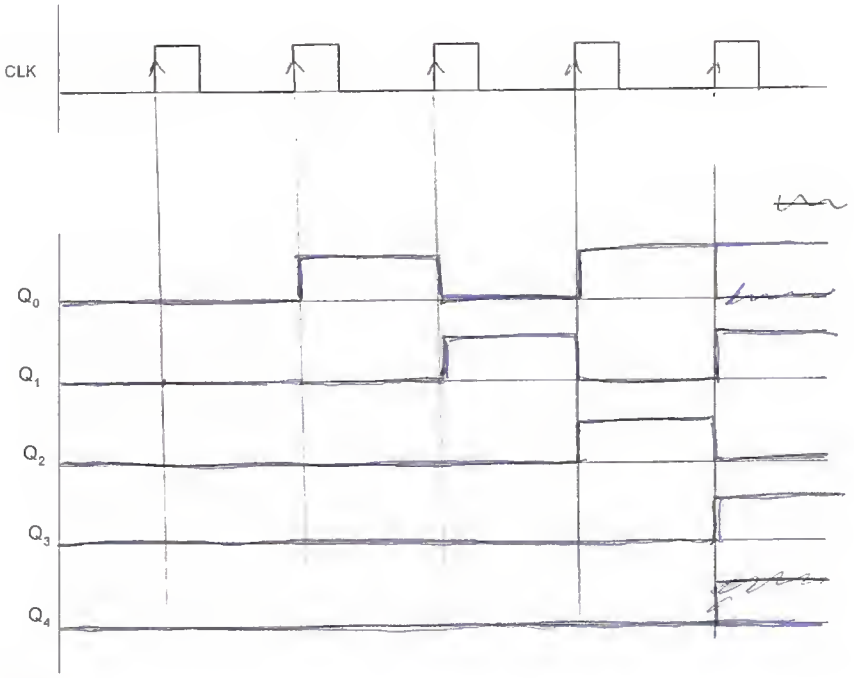
Question [4]: [25 mark]

For the 5-bit serial-in serial-out shift register, illustrate the entry of 11010.





Content:

1 - shifting at clock pulses only

2 - getting the idea of shifting to right.

3 - the data should be stored at 5th clock pule

4 - each change at asingle clock 5 munks But if maintainning the above 3 points 1, 2, 3